AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior listings of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Withdrawn) The semiconductor device of claim 1, wherein said first, second and third electrical interconnects and said surface are on a same side of said substrate, and said fourth electrical interconnect is on an opposite side of said substrate.

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Withdrawn) The semiconductor device of claim 8, further comprising a contact region formed on said substrate connecting said bottom gate region to said fourth electrical interconnect, said contact region being of said second conductive type at a concentration of at least 1E19 cm^{-3}.

10. (Withdrawn) The semiconductor device of claim 6, further comprising a top region of said first conductive type formed on said substrate between said surface and said top gate region,

thus forming a third *pn*-junction defining a third depletion region at a third depth relative to said surface, and an electrical interconnect in communication with said third depletion region for detecting a current therefrom.

11. (Withdrawn) The semiconductor device of claim 6, further comprising an additional top gate region of said second conductive type formed on said substrate adjoining said channel, thus forming a third *pn*-junction defining a third depletion region, and an electrical interconnect in communication with said third depletion region for detecting a current therefrom.

12. (Withdrawn) The semiconductor device of claim 11, wherein said top gate regions have different doping concentrations.

13. (Withdrawn) The semiconductor device of claim 11, wherein said third *pn*-junction is at a depth relative to said surface less than said first depth.

14. (Withdrawn) The semiconductor device of claim 6, wherein said channel comprises a buried region adjoining said bottom gate region forming said second *pn*-junction, said buried region having a doping concentration higher than that of said bottom gate region so that said second depletion region mainly develops within said bottom gate region.

15. (Withdrawn) The semiconductor device of claim 6, wherein said top gate region comprises a central region and a protective ring region around a periphery of said central region, said protective ring region having a higher doping concentration and being thicker than said central region.

16. (Withdrawn) The semiconductor device of claim 6, wherein said JFET is a first FET, and further comprising a second FET having a source, a drain, a channel of said second conductive type, and a gate of said first conductive type, said source region of said first FET connected to said source of said second FET, said drain region of said first FET being connected to said gate of said

second FET, said drain of said second FET being connected to a gate region of said first FET, thus forming a dual-FET device.

17. (Withdrawn) The semiconductor device of claim 16, wherein said FET is a JFET or a depletion-metal-oxide semiconductor FET (d-MOSFET).

18. (Withdrawn) The semiconductor device of claim 6, further comprising (i) one or more regions of alternating conductive types formed on said substrate extending from said bottom gate region away from said surface, thus forming one or more additional *pn*-junctions at different depths relative to said surface and forming one or more additional channels each between two adjacent *pn*-junctions; (ii) additional doped drain and source regions on said substrate in communication with each one of said one or more additional channels, respectively; and (iii) additional electrical interconnects in communication with said additional one or more *pn*junctions and said one or more channels, wherein said different depths are chosen to generate charge carriers in response to light of different wavelength bands incident on said surface respectively in said one or more regions, whereby incident light on said surface of said different wavelength bands are detectable through said additional source and drain regions, and said additional electrical interconnects.

19. (Withdrawn) A semiconductor device, comprising

a substrate having a surface;

a doped, photo-conductive channel of a first conductive type formed on said substrate beneath said surface, said channel having a bottom at a first depth relative to said surface,

doped drain and source regions formed on said substrate beneath said surface in communication with said channel, said source region having a bottom at a second depth relative to said surface, said drain region having a bottom at a third depth relative to said surface;

a doped gate region of an opposite, second conductive type formed on said substrate beneath and adjoining said channel and said source and drain regions, thus forming a *pn*-junction defining a depletion region;

said first depth chosen to generate charge carriers in said channel in response to light of a first wavelength band incident on said surface,

said second depth chosen to generate charge carriers in said depletion region proximate said bottom of said source region in response to light of a second wavelength band incident on said surface;

said third depth chosen to generate charge carriers in said depletion region proximate said bottom of said drain region in response to light of a third wavelength band incident on said surface;

first and second electrical interconnects in communication with said source and drain regions, respectively;

a third electrical interconnect in communication with said *pn*-junction;

whereby incident light on said surface at said first, second, and third wavelength bands are detectable through currents through said first, second, and third electrical interconnects.

20. (Withdrawn) The semiconductor device of claim 19, wherein said first depth is from 0.05 to 0.5 microns, said second depth is from 0.3 to 2 microns and said third depth is from 2 to 10 microns.

21. (Withdrawn) The semiconductor device of claim 19, wherein said first conductive type is n-type, said channel has a doping concentration of from about 1E15 to about 1E19 cm^{-3}, said source and drain regions having a doping concentration of about 1E20 cm^{-3}, and said gate region having a doping concentration from about 1E14 to about 1E15 cm^{-3}.

22. (Withdrawn) The semiconductor device of claim 19, further comprising one or more contact regions of said first conductive type formed within said channel distributed between said drain and source regions, said one or more contact regions having a higher doping concentration than said channel, and an electrical interconnect in contact with each one of said one or more contact regions for detecting an output signal therefrom.

23. (Withdrawn) The semiconductor device of claim 19, wherein a sub-region in said gate region adjoining said channel comprises a buried layer having a higher doping concentration than said channel so as to limit extension of said depletion region into said gate region.

24. (Withdrawn) The semiconductor device of claim 19, further comprising an oxide layer in contact with said channel and said drain region, a metal layer formed on said oxide layer thus forming a metal-oxide-semiconductor (MOS) gate, and an electrical interconnect in communication with said metal layer for detecting a current therefrom.

25. (Withdrawn) The semiconductor device of claim 19, further comprising an additional doped channel beneath said gate region and an additional doped gate region beneath said additional channel, doped source and drain regions in communication with said additional channel and an electrical interconnect in communication with said additional gate region for detecting currents therefrom respectively.

26. (Withdrawn) The semiconductor device of claim 25, further comprising source and drain regions in communication with said gate region between said channels for detecting a current between said source and drain regions through said gate region.

27. (Canceled)

28. (Cancelled)

29. (Withdrawn) The photo-sensing device of claim 28, wherein two or more of said plurality of photo-sensing units share either a common source region or a common gate region, or both.

30. (Withdrawn) The photo-sensing device of claim 28, wherein said plurality of photo-sensing units form a pattern for imaging.

31. (Withdrawn) The photo-sensing device of claim 28, wherein two or more of said photosensing units are stacked one below another.

32. (Currently Amended) A method of photo-sensing comprising:

biasing a junction field effect transistor (JFET) to generate a conducting channel between a source and a drain of said JFET, said conducting channel having an absorption section below a light-transmitting surface of said JFET, said absorption section having a pre-determined photo-conductivity spectral response, and

at least two depleted regions below said light-transmitting surface, each having a photo-electric spectral response peaking at a distinct, pre-determined wavelength;

illuminating said light-transmitting surface with light;

sensing an output signal derived from said channel indicative of the intensity of light absorbed therein; and

for each particular one of said depleted regions, sensing an output signal derived from said particular depleted region indicative of the intensity of light absorbed therein, wherein said one or more depleted regions comprise two depleted regions at different depths below said light-transmitting surface; wherein said sensing an output signal comprises sensing a drain-source current from said drain to said source through said conducting channel, and wherein said sensing an output signal derived from said particular depleted region comprises sensing a gate current from a gate in contact with said particular depleted region; and wherein said sensing a drain-source current comprises:

sensing a drain-source photo-induced current variation based on: sensing a drain current from said drain during said illuminating, obtaining a quiescent drain-source current, and calculating said photo-induced drain-source current variation by subtracting from said drain current said quiescent drain-source current and the sum of said gate currents.

33. (Cancelled)

34. (Cancelled)

35. (cancelled)

36. (cancelled)

37. (Previously presented) The method of claim 36, wherein obtaining a quiescent drain-source current comprises sensing a quiescent source current from said source and a quiescent drain current from said drain without illuminating said light-transmitting surface and calculating said quiescent drain-source current by subtracting said quiescent source current from said quiescent drain current.

38. (Currently Amended) The method of claim 37 ~~35~~, further comprising:

sensing a quiescent source current from said source regions in dark conditions,

sensing a source current from said source regions during said illuminating, and

calculating said photo-induced drain-source current variation by subtracting from said source current said quiescent source current.

39. (Previously Presented) The method of claim 32, wherein said pre-determined wavelengths are selected such that a plurality of different spectral components of said light can be determined from said output signals.

40. (Original) The method of claim 39, wherein said plurality of spectral components comprise a blue component, a green component and a red component.

41. (Original) The method of claim 40, wherein said blue component covers wavelengths below about 500 nm, said green component covers wavelengths from about 500 to about 600 nm, said red component covers wavelengths above about 600 nm.